Appendix N

Title: Receive/Transmit Port Interface V2.3.1

1 Introduction

1.1 Overview

The XPI block (macro name key: XI_) interfaces the serial data streams on e.g. PCM formatted IOs and maps them to/from chip internal processing. It therefore performs serial/parallel conversion and transfers data between the serial clock system and the on chip system clock.

The XPI contains the subfunctions RXPI for receive direction and TXPI for transmit direction.

1.2 Features

- serial interface operating with gapped/non gapped serial clocks
- operation with strobed serial clocks (**future extension**)
- standard channelized mode (SCM) : 28 T1 (1.544MHz) / E1 (2.048 MHz) lines with chip internal framing function
- alternate channelized mode (ACM) : 16 x T1 (1.544MHz) / E1(2.048MHz) lines **without** chip internal framing function (E1/T1 arbitrarily portwise programmable)
- unchannelized mode (UCM) and mixed modes (SCM/UCM or ACM/UCM), UCM mode available for 16 ports
- SCM test mode: processing of 9 bit test frames (in T1 mode only, ports #16-27 only)
- serial data sampling/transmitting with rising/falling edge of clocks (ACM, SCM and UCM)
- SCM: sampling the transmit sync puls with rising/falling edge of transmit clock
- Optional disable/enable of external transmit synchronization in SCM mode
- ACM: sampling the receive/transmit sync pulses with rising/falling edge of clocks
- ACM: programmable TD/RD bitshift of +3/-4 bits relative to the sync pulse
- serial data multiplexable between normal and internal loop input
- Looped timing: In SCM mode RCLK(n) can be chosen as clock source for the transmit part of port#n
- supervision of frame synchronization conditions
- Signaling of the On Chip Framer receive synchronization for one port out of 28(SCM) at the serial interface or, alternatively, signaling of the effective transmit clock of port#0
- PCM-, HDLC-, framer- and interrupt-interface
- performance: serial clock up to 20MHz (port 0: 60MHz) ; SYSCLK up to 70 MHz
  (in M256F application only the port 0 provides a data rate up to 60 MBit/s)
- number of gates:
- area:
- power consumption:

- full scan path for the sysclk domain (in M256F no scan path for serial clock domains)

1.3 System Integration

RXPI interfaces:

- n serial PCM interfaces [M256F: n=28]
- one parallel (8bit data + 5bit timeslot number) REQ/GNT interface to TSAR arbiter (provides receive data and corresponding timeslot information)
- n single bit interfaces [M256F: n=28] to the FRAMR (provides framer data)

TXPI interfaces:

- n serial PCM interfaces [M256F: n=28]
- one parallel (8bit data + 8bit mask + 5bit timeslot number) REQ/GNT interface to TSAT arbiter (provides timeslot information for selected port)
- n single bit interfaces [M256F: n=28] to the FRAMT (provides framer data and transmit sync pulse)

Shared interfaces:

- one FPI Slave (TFPI) Bus
- one Interrupt Bus

The RXPI subblock is used at the chip interface, in order to prepare the serial data for further processing. The PCM data is sampled with its respective clock and synchronized to the system clock domain. The frame alignment and DL support is provided by the framer receive part (FRAMR interface). The data provided with corresponding port and timeslot information is transferred to the timeslot assigner (TSAR interface).

The TXPI subblock is used to make serial transmit data available at the PCM interface. The data which are received from the TSAT macro, 8 bit in parallel, is composed to the desired frame and hyperframe structure. The DL and framing information is provided by the framer transmit part (FRAMT interface). The transmit data is transferred from the system clock domain to the PCM transmit clock domains of the corresponding ports.

Configuration of the RXPI and TXPI is done via slave accesses to the TFPI interface. Interrupt conditions are flagged by writing interrupt vectors to the interrupt interface.

One RXPI#n and one TXPI#n subblock corresponds to one serial interface. Up to 32 instances of the RXPI#n and TXPI#n can be combined to form the block RXPI and TXPI, respectively.

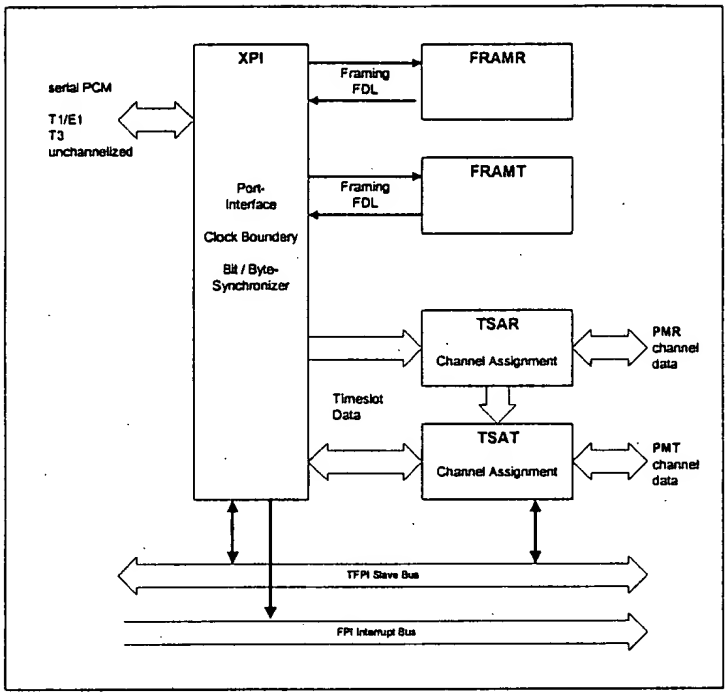


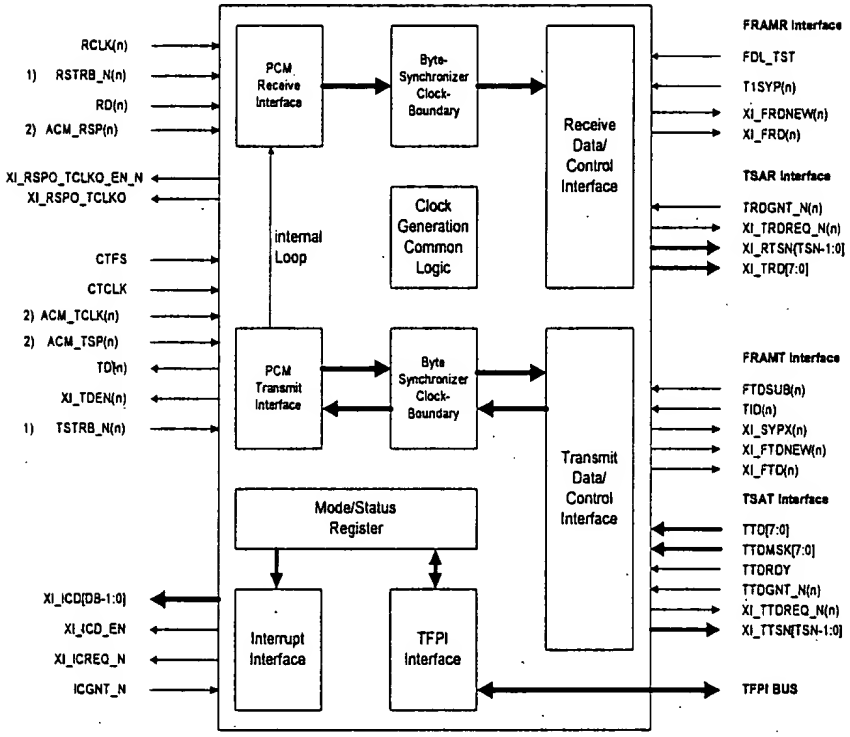
Figure 1.3: System Integration

1.4 Known Restrictions

1) For synchronization purposes, the frequency ratio SYSCLK / RCLK(TCLK) must be at least 3.5 : 1 for the ports #1 - 15, i.e. the max. RCLK(TCLK) frequency in UCM is approximately 9 MHz, provided that SYSCLK frequency = 33 MHz. Maximum serial frequency of the ports#16-27 is 2.048 MHz, regardless of the operation mode.
2) For unchannelized mode (UCM) all timeslots of a port have to be assigned to one channel. In UCM the XPI macro generates the T1 time slot scheme, i.e. 24 time slots (round robin) are given to the TSA.

2 Functional Description

2.1 XPI Block Diagram



Note 1): for M256F application fixed to "0"
Note 2): for M256F application ACM mode for port#n = 0...15 only

Figure 2.1: XPI Block Diagram

2.2 Normal Operation Description / Reset RXPI and TXPI

After HW or SW reset all registers are set to the benign state. There is no difference between HW and SW reset concerning the effect on the XPI hardware. The interface mode will be set to: 28xT1 (SCM) as defined by the reset value of the global configuration register **CONF1.GPM** .

Receive Direction:

All receive lines are disabled by the reset status of the receive enable register **XPI.REN[31:0]** = 00000000_H. Each bit of register REN corresponds to the respective receive port. No requests to TSAR and FRAMR are generated in this state, however the corresponding data bits at these interfaces have defined values ('0').

Start of operation is achieved by programming a REN bit to '1'. In SCM mode the requests to the FRAMR will start, but requests to TSAR will not start until the FRAMR indicates the synchronous state to (R)XP.

If the general port mode has been programmed to ACM (16 T1/E1 ports) by the register **CONF1.GPM** (simultaneously for the complete XPI !), the ports 0 to 15 expect the sync signal not to come from FRAMR, but from the macro input ACM_RSP(0...15). In this mode REN enables/disables only requests to TSAR. Requests to the FRAMR are generally disabled in ACM mode. Synchronization is achieved when two conditions are valid:

a) enabling of a port by setting the corresponding REN bit to '1';

b) at least one external receive sync pulse on ACM_RSP(n) has arrived to trigger the XPI timeslot counter. The timeslot counter is sensitive to RSP immediately after the reset lines are switched inactive, independent of an active or inactive REN.

After the synchronous state is achieved, the (R)XPI generates requests to the TSAR. If TSAR is still in stop mode or set to inhibit (timeslot), the requests are granted but discarded inside TSAR.

Transmit Direction:

In transmit direction the transmit enable register **XPI.TEN[31:0]** is also reset to 00000000_H, thus tristating the corresponding output ports. Each bit of the register TEN corresponds to the respective transmit port. The default interface mode is 28xT1 as defined by the reset value of GPM.

No requests to TSAT and FRAMT are generated in this state, however the corresponding data bits at these interfaces have defined values ('0'). When a bit TEN for

a port is set to '1' and additionally, the transmit timeslot counter is triggered by at least one external trigger event ,(T)XPI has achieved the synchronous state.

With the next external trigger event, the (T)XPI will start requests to FRAMT and TSAT. If TSAT is still in stop mode or set to inhibit (timeslot), the requests are granted and answered to (T)XI with mask bit field set to '0' (all bits disabled).

The TXPI sends the data received from TSAT on the PCM line for this port. In SCM mode, the transmit timeslot counter is sensitive on CTFS which synchronizes all of the 28 ports (exception: looped timing and CTFS disable, s. section "Looped Timing" below).

If the general port mode has been programmed to ACM (16 xT1/E1) (ACM) via GPM (simultaneously for the complete XPI !), the ports 0 to 15 expect the sync signal not to come from CTFS input pin, but from the macro input ACM_TSP(0...15). In this mode TEN enables/disables only requests to TSAT. Requests to the FRAMT are generally disabled in ACM mode. The transmit clocks are provided via ACM_TCLK(0...15).

Receive/Transmit Direction:

All ports , which are activated (28 in SCM or 16 in ACM), can be selected separately to operate in unchannelized mode, by appropriate programming the port mode register **(XPI.PMR)**. Physically, there exists one port mode register for each port.
In unchannelized mode no requests to the framer are generated from the respective ports.The unchannelized mode performs transparent data transfer without frame alignment. The framer function and any synchronization supervision is disabled in this mode. In UCM the XI macro generates the T1 time slot scheme, i.e. 24 time slots (round robin) are given to the TSA.

All interrupts generated by the ports (sync/async interrupts) are masked after reset, since the reset value of port mode register bit TEIM and REIM (transmit/receive sync error interrupt mask) is set to '1' (s. section "Port Interrupts").

After reset CTCLK is selected as global transmit clock for all output ports due to the reset value of CONF1.GPM = 0 (SCM mode, s. Figure 2.2.a). After switching to ACM mode (GPM = '1') each transmit clock domain #n (n = 0..15) is driven by the corresponding transmit clock ACM_TCLK(n). In the non loop case, each receive clock domain #n is clocked by the corresponding receive clock rclk(n) (n = 0..28 for SCM, n = 0..15 for ACM).

An internal test loop (TD out-> RD in XPI) is activated by programming the register CONF2 setting ILP to '1'. The loop function is available for only one port at a time, the port number being defined by CONF2.LPPID[4:0]. The respective transmit data and the transmit strobe information is sent to the corresponding receive port. In SCM mode, the receive part of the loop port is clocked by CTCLK. The on chip framer provides the receive frame synchronization. In ACM mode, the receive clock for the loop port #n (n =

0...15) is generated from the respective transmit clock, ACM_TCLK(n) (s. clock multiplexer, Figure 2.2.b). The receive frame synchronization corresponds to the transmit synchronization which is triggered by ACM_TSP(n).

For test purposes, the receive synchronization info provided by the on chip framer is visible on XI_RSPO_TCLKO for one port at a time. This test function is enabled by setting CONF2.RSPEN to '1'. The sync pulse is visible with a latency of 1 frame. The port selection is done via CONF2.SPAD(4:0). If CONF2.RSPEN is reset to '0' the effective transmit clock of port #0 is visible on XI_RSPO_TCLKO.

PCM Tristate Handling (Transmit Direction)

SCM mode, T1/E1: During and after an active sw or hw reset the PCM transmit data lines are tristated. When the transmit enable register (TEN) is enabled and the synchronous TXPI state is achieved, the first non tristate bit on the PCM data line is the first bit requested from TSAT. Mask information coming from TSAT is ignored, i.e. even data bits accompanied by active mask bits are driven actively on the PCM line. One or two transmit clock cycles after TEN is disabled, the PCM data line is switched to tristate.

UCM mode in case CONF1:GPM = 0: Apart from the fact that a synchronization phase does not exist, the tristate handling is the same as in T1/E1 mode.

ACM mode, T1/E1: The tristate behaviour is identical to the behaviour in SCM mode with the exception that data bits masked by TSAT are tristated.

UCM mode in case CONF1:GPM = 1: The tristate behaviour is identical to the behaviour in UCM mode (CONF1:GPM = 0) with the exception that data bits masked by TSAT are tristated. However, in UCM mode TSAT mask bits should be generally avoided.

Looped Timing

In SCM mode, the clock source for the transmit part of port#n (n = 0, ... , 27) can be switched from CTCLK to the corresponding receive clock RCLK(n), setting PMR.LT of port#n to '1'. An arbitrary subset of the transmit ports can be switched to looped timing. In case of an activated looped timing, the external receive frame synchronization via CTFS is disabled, i.e. the transmit frame counters are no longer triggered by CTFS pulses; they are free running. The supervision of the transmit synchronization is suspended (s. section "Port Interrupts").

The suspension of the external transmit frame synchronization incl.sync-async interrupt generation can also be achieved by setting PMR:CTFSD to '1'. However, in case of

PMR.CTFSD = '1' and PMR.LT = '0', the serial transmit part is operating with the regular SCM transmit clock CTCLK.

FDL Test Mode

For FDL test reasons a short frame test mode is implemented to yield higher F-bit data rates in order to reduce FDL verification effort. This test mode can be activated only for the ports #16 to #27 (SCM only ports), provided that

a) the dedicated XPI input pin FDL_TST is set to '1',

b) CONF1.GPM = '0' (SCM mode)

c) PMR.PCM = "0000" (T1 mode) for the enabled ports.

In short frame mode, the frame length is 9 bit, bit #0 treated as the framing bit. Apart from the frame length, the complete frame processing is the identical to the regular T1 SCM frame processing.

Port Interrupts

Port interrupts indicate the synchronous or asynchronous state of a port. Immediately after enabling the port interrupts by resetting the interrupt mask bits, port interrupts are generated indicating the current sync or async states. After this initial interrupt generation, a further interrupt occurs only when the state of a port changes from sync to async or vice versa. The reset value of the receive and transmit port state is async.

State Transitions

a) Standard Mode

A transmit port changes to the synchronous state, if common transmit frame synchronization is enabled and the number of bits between two synchronization pulses is equal to the number of frame bits of the selected mode or is equal to a multiple of that number. Immediately after reset, already the first CTFS pulse causes the transmitter to change to the synchronous state.

In case the common transmit frame synchronization is disabled, i.e. the looped timing bit or the CTFS disable bit of a port is set in PMR, the initial asynchronous state will not be left.

A transmit port changes to the asynchronous mode if the number of bits between two synchronization pulses is not equal to a multiple of the number of frame bits of the selected mode.

A receive port changes to the synchronous state, if the number of bits between two synchronization pulses generated by the port related framer is exactly equal to the

number of frame bits of the selected mode. Immediately after reset, already the first framer pulse causes the receive port to change to the synchronous state.

A receive port changes to the asynchronous state if the number of bits between two framer synchronization pulses is not equal to the number of frame bits of the selected mode. The receive port expects an on-chip framer sync pulse for each frame.

b) Alternate Mode

A port changes to the synchronous state if the number of bits between two synchronization pulses is equal to a multiple of the number of frame bits of the selected mode. Immediately after reset, already the first synchronization pulse causes the port to change to the synchronous state. This holds for both directions, receive and transmit.

A port changes to the asynchronous state if the number of bits between two synchronization pulses is not equal to a multiple of the number of frame bits of the selected mode (receive and transmit direction).

In general, a state transition occurs only in T1 and in E1 mode. In unchannelized mode no supervision of frame synchronization is performed. The initial asynchronous state will not be left.

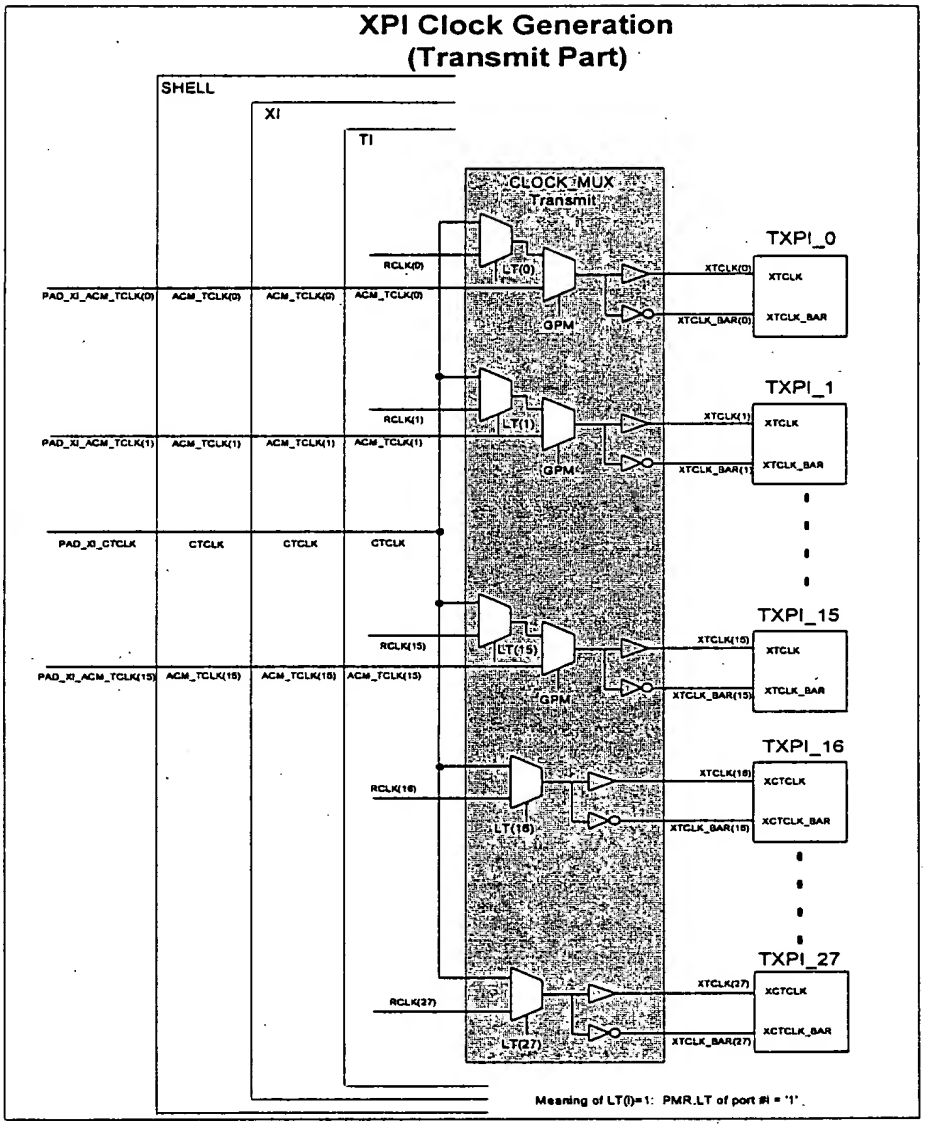


Figure 2.2a:
XPI Transmit Clock Generation

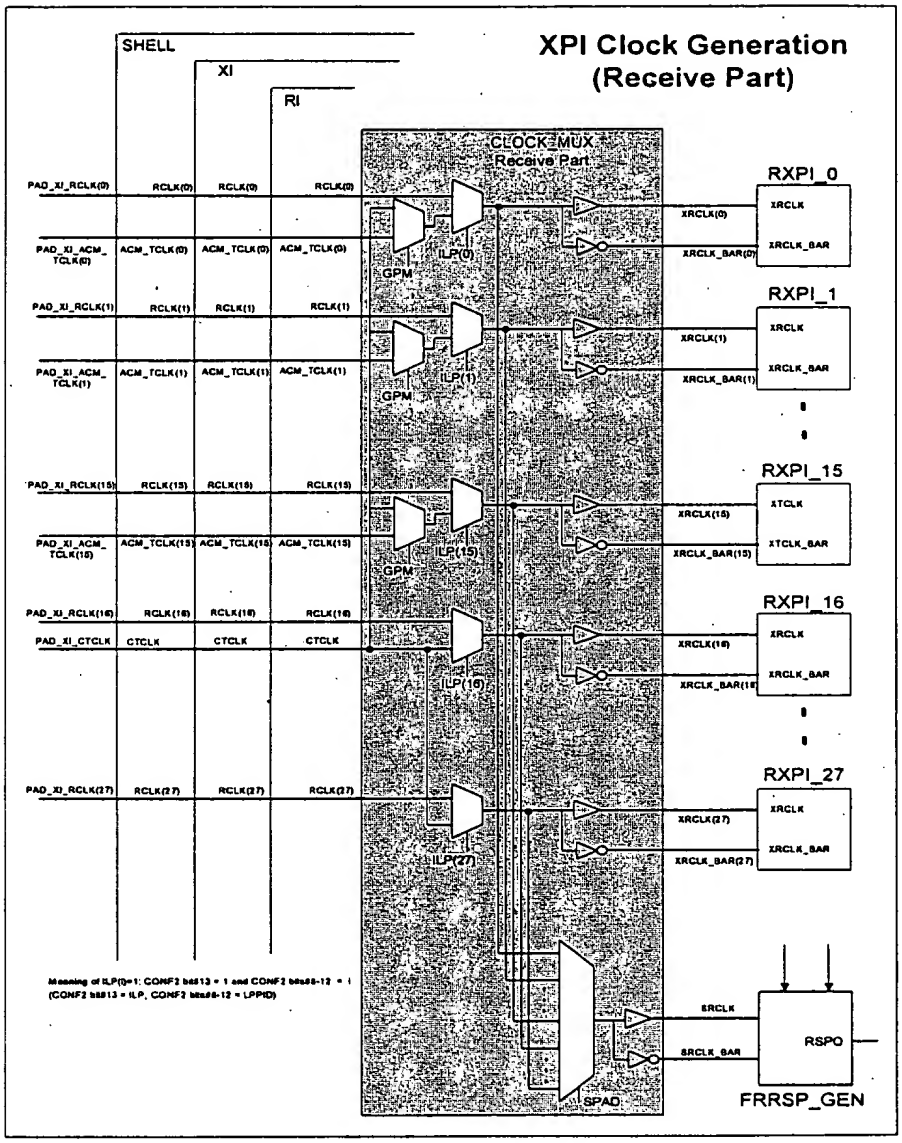


Figure 2.2b:
XPI Receive Clock Generation

3 Macro Interfaces and Signal Description

All signals are active high until otherwise specified. Active low signals are designated by "_N" appended to their names. To make the design as re-usable as possible, a bus signal whose width is application dependent is specified with one of the following parameters:

Parameter name	Bus Type	Typical Value (Bits) M256F
PN	max. port number	28
TSN	max. timeslot number bus	5
PAD	port address	5
ICD	max. interrupt vector	10
DB	data bus width	32
AB	address bus witdth	32

3.1 (Bus-) Interfaces and Protocols

3.1.1 Global Signals

Signal Name	Direction	Type	Tsu/Thld Td	meaning/comment special characteristics
SYSCLK	i			System Clock
HW_RESET_N	i			Hardware Reset
SW_RESET_N	i			Software Reset
SCANMODE	i			Scan Test Mode
M256_MODE	i			Switch to hardwired ACM mode

3.1.2 Timeslot Assigner Receive Interface

The TSAR interface consists of the following signals:

Signal Name	Direction	Type	Tsu/Thld Td	meaning/comment special characteristics
TRDGNT_N[PN-1:0]	i			data/tsnum bus is granted to port n=index
XI_TRDREQ_N [PN-1:0]	o			request from port n=index for servicing/reading 8 bit data
XI_TRD[7:0]	o			data bus containing 8 bit serial/parallel converted time slot data (bit 0 is the first serial bit received, bit 7 is the last serial bit received)
XI_RTSN[TSN-1:0]	o			time slot bus containing the time slot number of the corresponding data XI_TRD (valid time slot numbers are 0 to 23 for T1, 0 to 31 for E1 . **For unchannelized mode all timeslots of a port have to be assigned to one channel. In UCM the XPI macro generates the T1 time slot scheme, i.e. 24 time slots (round robin) are given to the TSA.**

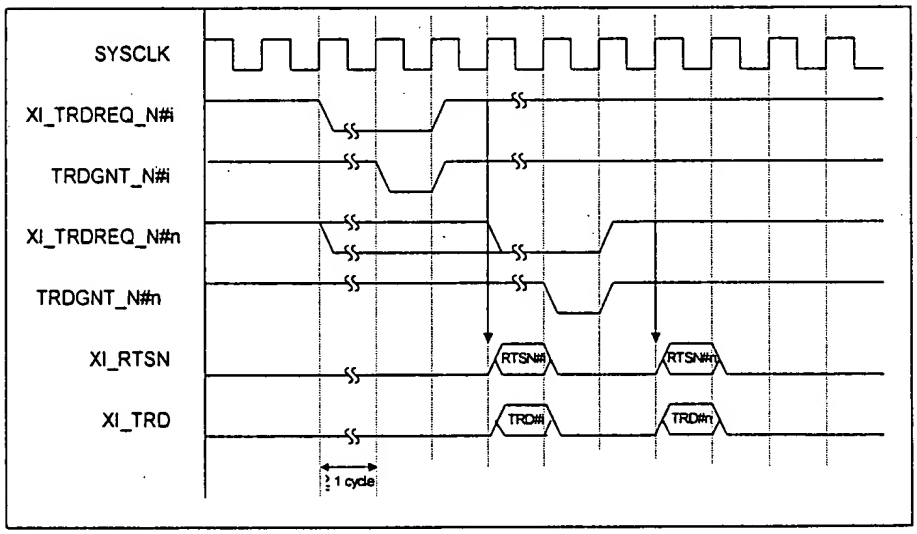


Figure 3.1.2:

TSAR Interface Timing Diagram

Description of TSAR interface protocol:

As soon as any port RXPI[n] has 8 bit data available for processing, it asserts the signal XI_TRDREQ_N to the arbiter part of the TSAR, in order to request service. The arbiter then grants TRDGNT_N the respective port access to the busses XI_TRD (data) and XI_RTSN (time slot number). TRDREQ_N is deasserted to indicate valid data on the busses XI_TRD and XI_RTSN. TSAR reads the bus information and deasserts TRDGNT_N.

The XI_RTSN and XI_TRD busses are generated by multiplexers which select the data of port#n according to TRDGNT_N#n. As a consequence, combinatorial delays are generated that may not be allowed application specifically (e.g. M256F).Therefore, the timeslot and data busses have to be registered within the macro (one additionally waitstait to TSAR).

3.1.3 Framer Receive Interface

The FRAMR receive interface consists of the following signals:

Signal Name	Direction	Type	Tsu/Thld Td	meaning/comment special characteristics
XI_FRDNEW[PN-1:0]	o	p * 1.		new receive data bit is valid (one signal per port)
XI_FRD[PN-1:0]	o			framer receive data (one bit per port)
T1SYP[PN-1:0]	i			framer receive control signal, to be evaluated when XI_FRDNEW is asserted, timeslot count and supervision of frame synchronization condition is triggered (s. Table 3.1.3)
FDL_RX_TST	i			If set to '1', the short frame test mode is active in SCM T1 mode

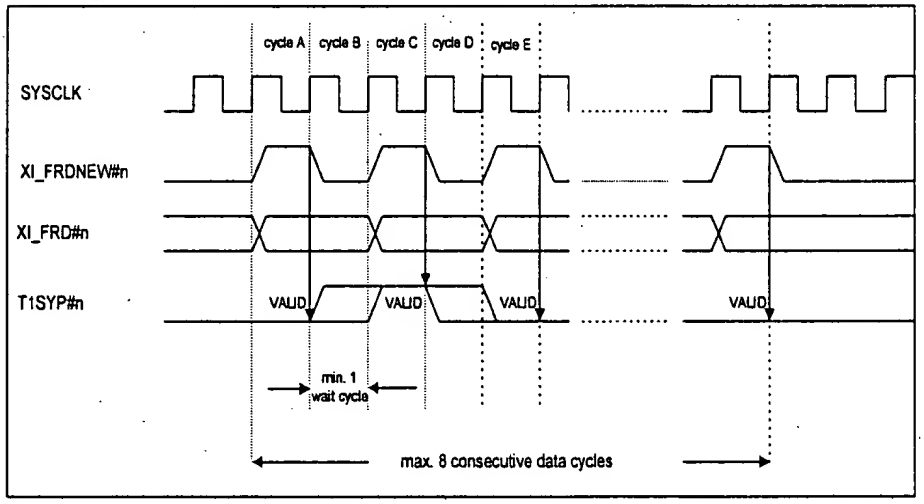


Fig. 3.1.3:
FRAMR interface timing diagram

Description of FRAMR interface protocol:

Each of the 28 PCM ports has its dedicated set of framer control and data signals. Fig.3.1.3 shows the signalling of one of the 28 port specific protocols which are driven completely independent.

Cycle A

A one cycle pulse on new bit indication signal (bit #n of XI_FRDNEW) is activated to request frame processing for the serial data bit of port #n, available on XI_FRD#n. The framer status signal T1SYP#n is sampled in response to the new bit indication. T1SYP#n must always be valid for each pulse of XI_FRDNEW#n.

Cycle B

A minimum of one wait cycle is performed before the next activation of XI_FRDNEW. At this time T1SYP#n is don't care for the XPI macro.

Cycle C

The next pulse of XI_FRDNEW is activated to request frame processing for the serial data bit of port #n, available on XI_FRD#n. T1SYP#n is sampled in response to the new bit indication. Table 3.1.3 shows the relevant signal combinations:

XI_FRDNEW	T1SYP	
1	0	T1 and E1: the current bit is to be passed to TSAR
1	1	T1: data to be deleted (frame bit# 0). The timeslot count and supervision of frame synchronization condition is triggered . E1: the current bit is to be passed to TSAR + sync check
0	x	no action

Table 3.1.3

Cycle D

A minimum of one wait cycle is performed before the next activation of XI_FRDNEW#n. At this time T1SYP#n is don't care for the XPI macro.

Cycle E

The next pulse of XI_FRDNEW#n is activated to request frame processing for the serial data bit of port #n, available on XI_FRD#n. At this time T1SYP#n must be updated.

Because of bytewise data processing, a maximum of 8 consecutive data cycles are possible in the worst case. However, the bytewise data processing is performed only for port#0 which has to meet high speed conditions. The ports no. 1 - 27 request frame processing only once in serial clock cycle (M256F application).

3.1.4 Timeslot Assigner Transmit Interface

The TSAT interface consists of the following signals:

Signal Name	Direction	Type	Tsu/Thld Td	meaning/comment special characteristics
XI_TTDREQ_N[PN-1:0]	o			request from transmit port n=index for servicing/ reading 8 bit data and 8 bit mask field
XI_TTSN[TSN-1:0]	o			time slot bus containing the time slot number for the data TTD and mask TTDMSK (valid time slot numbers are 0 to 23 for T1, 0 to 31 for E1 **For unchannelized mode all timeslots of a port have to be assigned to one channel. In UCM the XPI macro generates the T1 time slot scheme, i.e. 24 time slots (round robin) are given to the TSA.**
TTDGNT_N[PN-1:0]	i			XI_TTSN bus is granted to transmit port n=index
TTDRDY	i			TSAT has finished data transfer in current clock cycle
TTD[7:0] TTDMSK[7:0]	i			data bus containing 8 bit time slot data and 8 bit mask bit field

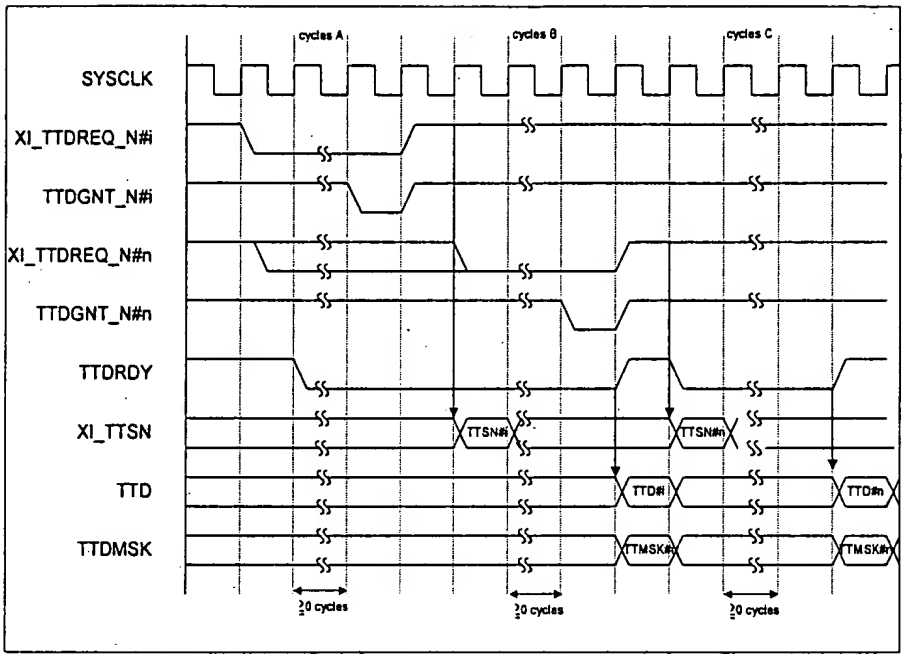


Figure 3.1.4:

TSAT Interface Timing Diagram

Description of the (T)XPI interface protocol:

As soon as any port TXPI[n] needs 8 bit data for transmit, it asserts the request signal XI_TTDREQ_N to the arbiter part of the TSAT, in order to request service. The arbiter then grants TTDGNT_N the respective port access to the bus XI_TTSN (transmit time slot number). XI_TTDREQ_N is deasserted to indicate valid data on the bus XI_TTSN. TTDRDY is asserted to indicate that the current data transfer has finished and valid data on the busses TTD and TTDMSK are available.

Each of the cycles A, B and C represents one or more clock cycles or it may be removed completely from the timing diagram.

The XI_TTSN bus is generated by a multiplexer which selects the data of port#n according to TTDGNT_N#n. As a consequence, combinatorial delays are generated that may not be allowed application specifically (e.g. M256F). Therefore, the timeslot bus has to be registered within the macro (one additionally waitstate to TSAT).

3.1.5 Framer Transmit Interface

The FRAMT transmit interface consists of the following signals:

Signal Name	Direction	Type	Tsu/Thld Td	meaning/comment special characteristics
XI_SYPX[PN-1:0]	o	p * 1		synchronous pulse transmit, to be evaluated when XI_FTDNEW is asserted (synchronized input CTFS)
XI_FTDNEW[PN-1:0]	o	p * 1		new transmit data bit is valid (one signal per port)
XI_FTD[PN-1:0]	o			framer transmit data, (one bit per port)
FTDSUB[PN-1:0]	i			framer transmit control signal, to be evaluated when XI_FTDNEW is asserted (s. Table 3.1.6)
TID[PN-1:0]	i			framer data to be inserted
FDL_TX_TST				If set to '1', the short frame test mode is active in SCM T1 mode

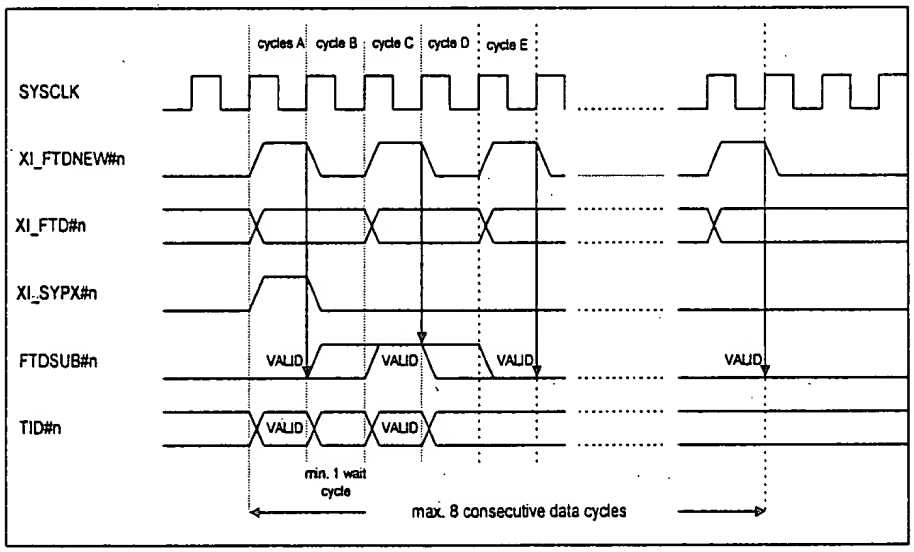


Fig.3.1.5:
FRAMT Interface Timing Diagram

Description of FRAMT interface protocol:

Each of the 28 PCM ports has its dedicated set of framer control and data signals. Fig.3.1.5 shows the signalling of one of the 28 port specific protocols which are driven completely independent.

The new bit indication line (bit #n of XI_FTDNEW) is activated to request frame processing for the serial data bit of port #n, available on XI_FTD#n.

Cycle A

A one cycle pulse on the new bit indication signal XI_FTDNEW#n is activated to request frame processing for the serial data bit of port #n, available on XI_FTD#n. FTDSUB#n coming from the framer is sampled in response to the new bit indication. FTDSUB#n must always be valid for each pulse of XI_FTDNEW#n.

An additionally activated XI_SYPX#n triggeres the FRAMT timeslot counter to indicate the beginning of a new frame. XI_SYPX marks bit #0 (F-bit or DL-bit) of the current frame which consists of 193 bits in T1 mode, resp. 256 bits in E1 mode. Table 3.1.5 shows the relevant signal combinations.

Cycle B

A minimum of one wait cycle is performed before the next activation of XI_FTDNEW. At this time FTDSUB#n and TID#n is don't care for the XPI macro.

Cycle C

The next pulse of XI_FRDNEW#n is activated to request frame processing for the serial data bit of port #n, available on XI_FTD#n.

The status signal FTDSUB is sampled in response to the new bit indication. Table 3.1.5 shows the relevant signal combinations:

XI_FTDNEW	XI_SYPX	FTDSUB	
1	0	0	data ready for PCM bit stream
1	0	1	required data has to be substituted by TID#n (e.g. test data coming from the framer)
1	1	0	sync bit location (F-bit), The framing bit or DL bit or CRC bit has to be provided on TID#n. The current data bit XI_FTD#n is postponed. Only used in T1 mode

XI_FTDNEW	XI_SYPX	FTDSUB	
1	1	1	sync check; data has to be substituted by TID#n. Only used in E1 mode bit #0.
0	x	X	no action

Table 3.1.5

Cycle D

A minimum of one wait cycle is performed before the next activation of XI_FTDNEW#n.

Cycle E

The next pulse of XI_FTDNEW#n is activated to request frame processing for the serial data bit of port #n, available on XI_FTD#n. At this time the status signal FTDSUB coming from the framer must be updated.

Because of bytewise data processing, a maximum of 8 consecutive data cycles are possible in the worst case. However, the bytewise data processing is performed only for port#0 which has to meet high speed conditions. The ports no. 1 - 27 request frame processing only once in serial clock cycle (M256F application).

3.1.6 Interrupt Interface

The interrupt controller interface consists of the following signals:

Signal Name	Direction	Type	Tsu/Thld Td	meaning/comment special characteristics
ICGNT_N	i			XPI is granted to interrupt bus
XI_ICREQ_N	o			request from XPI for interrupt servicing
XI_ICD[ICD-1:0]	o			interrupt bus (vector)
XI_ICD_EN	o			interrupt bus data enable

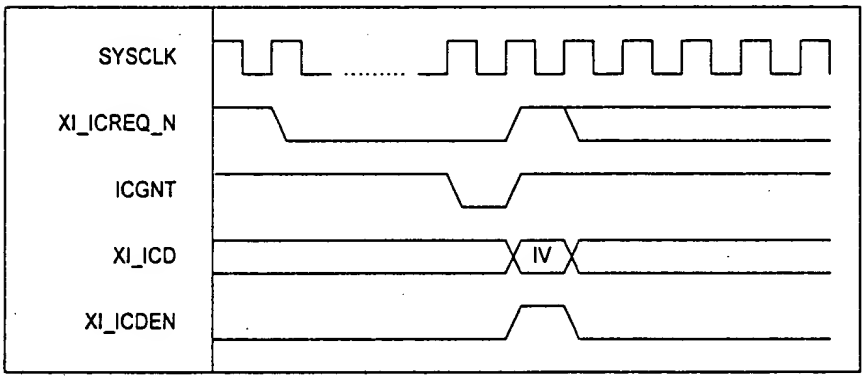


Figure 3.1.6:
Interrupt Controller Interface

Description of interrupt interface protocol:

XI activates XI_ICREQ_N to indicate an interrupt vector on XI_ICD. Data are valid in the next clock after ICGNT_N active. The XI could generate an asyc/sync interrupt at any PCM frame. For M256F application max. 56 interrupts (28 tx, 28 rx) are possible at a time.

Receive/Transmit Interrupt Vector

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	0	TDIR	0	Q2	Q1	Q0	0	0	0	0	0	0	SYN	ASYN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	PORT[4:0]				

TDIR:
direction ('1': transmit; '0': receive)

Q(2:0):
queue number for interrupt vector (refer to register **CONF2** bit PORTIQ[2:0])

SYN
Synchronous state indication
SYN interrupts are generated
1) immediately after enabling the interrupts by resetting the interrupt mask bits when the port is in synchronous state (initial interrupt) or
2) in case the state changes from async to sync.

ASYN
Asynchronous state indication
ASYN interrupts are generated
1) immediately after enabling the interrupts by resetting the interrupt mask bits when the port is in asynchronous state (initial interrupt) or
2) in case the state changes from sync to async.

PORT(4:0):
port number for which the interrupt vector (IV) is written

3.1.7 FPI Target Interface

In the following sections, "Flexible Peripheral Interconnect (FPI) Bus compliant" means that the specified bus uses a subset of the FPI features and satisfies the basic address and data cycle. Not all FPI signals are implemented because default values are sufficient for the application i.e. they can be coded as constants in the hardware. Refer to the FPI bus specification and FPI + Target Template Bus for details of the complete bus.

The FPI Target interface consists of the following signals:

Signal Name	Direction	Type	Tsu/Thld Td	meaning/comment special characteristics
TFPI_RD_N	i			Read control
TFPI_WR_N	i			Write control
TFPI_A[AB-1:2]	i			Address bus
TFPI_D[DB-1:0]	i			Data bus, valid during write transfer
TFPI_RDY	i			End of transfer indicator
VG_TFPI_SEL_N	i			(Macro) select input (broadcast programming virtual global register)
TFPI_SEL_N	i			(Macro) select input (macro specific programming)
XI_TFPI_D[DBB-1:0]	o			Data bus, active during read transfer
XI_TFPI_D_EN	o			Data Enable
XI_TFPI_RDY	o			Ready Output
XI_TFPI_RDY_EN	o			Ready Enable

3.1.8 PCM Interface

The PCM interface consists of the following signals:

Signal Name	Direction	Type	Tsu/Thld Td	meaning/comment special characteristics
XI_RSPO_TCLKO	o			carries the receive synchronization info provided by the on chip framer for a user selectable port, if CONF2.RSPEN = 1. Each framer sync pulse is visible on XI_RSPO_TCLKO with a delay of 1 frame. If CONF2.RSPEN = 0, the effective transmit clock of port #0 is visible on XI_RSPO_TCLKO
CTFS	i			Common Transmit Frame Sync Signal This signal is used to synchronize the transmit lines that are clocked with CTCLK in SCM mode
RSTRB_N[27:0]	i			Strobe indicating valid receive data, the strobe signal is valid along the corresponding receive data RD
TSTRB_N[27:0]	i			Strobe indicating valid transmit data. The strobe signal is expected to be provided half a clock cycle before the corresponding transmit data XI_TD is generated.
CTCLK	i			Common Transmit Clock Reference Input
XI_TD[27:0]	o			Transmit Data DS1 Port 0..27
ACM_TCLK[15:0]	i			ACM Transmit clock for ports 0-15
RCLK[27:0]	i			Receive Clock for ports 0-27
RD[27-0]	i			Receive Data for ports 0-27
ACM_TSP[15:0]	i			ACM Transmit Frame Sync Signal for ports 0-15
ACM_RSP[15:0]	i			ACM Receive Frame Sync Signal forpPorts 0-15
XI_RSPO_EN	o			Pad Enable for XI_RSPO
XI_TDEN[27:0]	o			Tristate Control for Transmit Data

Refer to the Implementation Specification M256F for details of the complete interface. Operation with strobed serial clocks is for future extension and not relevant for the M256F application.

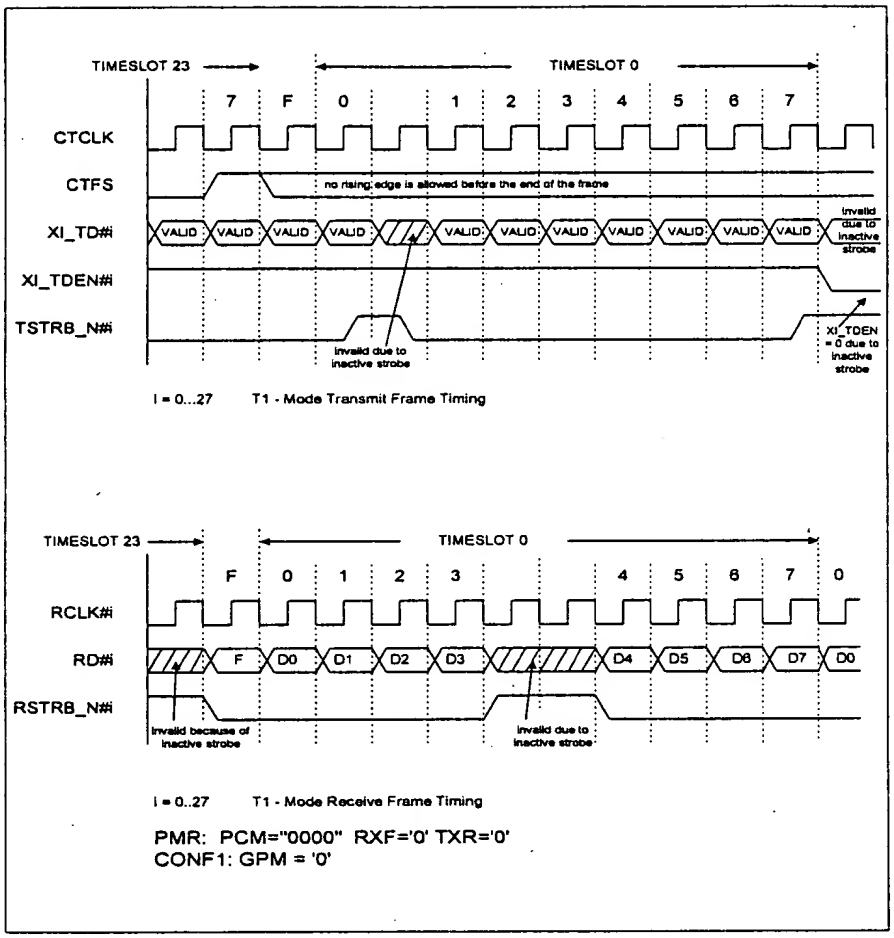


Figure 3.1.8a:

PCM interface timing for SCM: T1 with internal framing function

Port mode register (PMR): RXF = 0, TXR = 0 (LT = CTFSD = 0)

Transmit: generation of transmit data at falling CTCLK edge, sampling of the transmit sync pulse CTFS at rising edge, sampling of the transmit strobe TSTRB_N at falling CTCLK edge (TSTRB_N is provided half a clock cycle before the corresponding data is generated).

Receive: sampling of the receive data and receive strobe at rising RCLK edge.

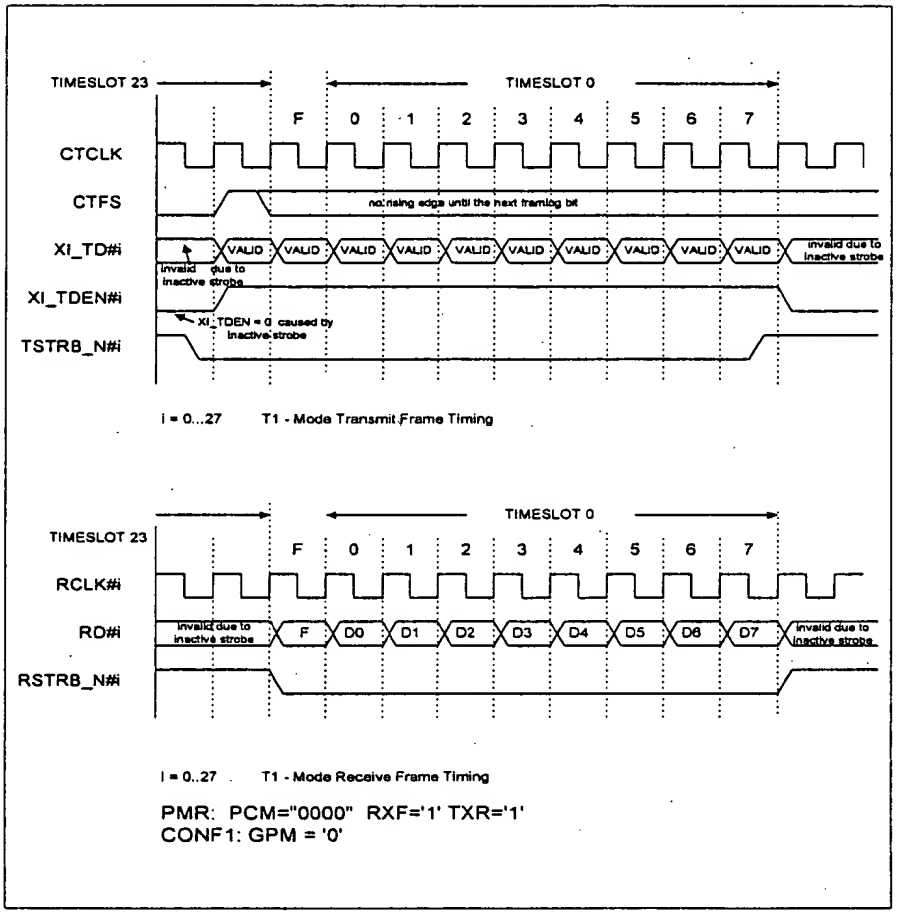


Figure 3.1.8b:

PCM interface timing for SCM: T1 with internal framing function

Port mode register (PMR): RXF = 1, TXR = 1 (LT = CTFSD = 0)

Transmit: generation of transmit data at rising CTCLK edge, sampling of the transmit sync pulse CTFS at falling edge, sampling of the transmit strobe TSTRB_N at rising CTCLK edge (TSTRB_N is expected to be provided half a clock cycle before the corresponding data is generated).

Receive: sampling of the receive data and receive strobe at falling RCLK edge.

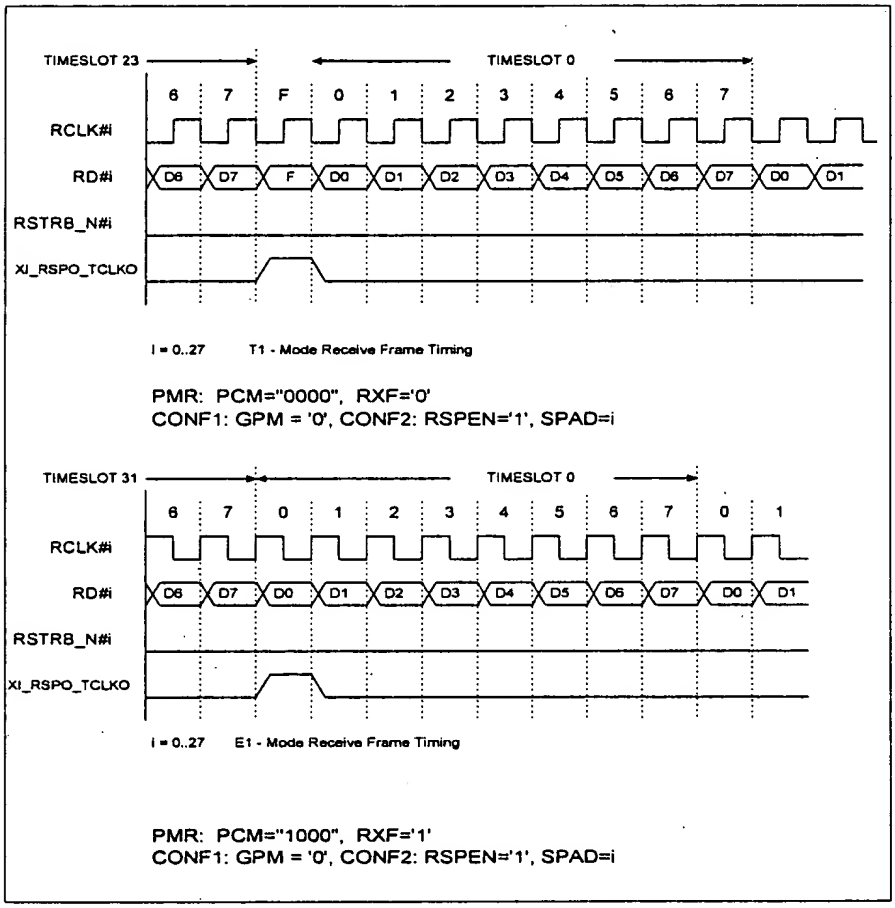


Figure 3.1.8c:

PCM interface timing for SCM: T1, E1 with internal framing function

XI_RSPO_TCLKO carries the receive synchronization info provided by the on chip framer for a user selectable port. The sync pulses are visible after the framer has reached its synchronization state. This test function requires an always activated receive strobe RSTRB_N

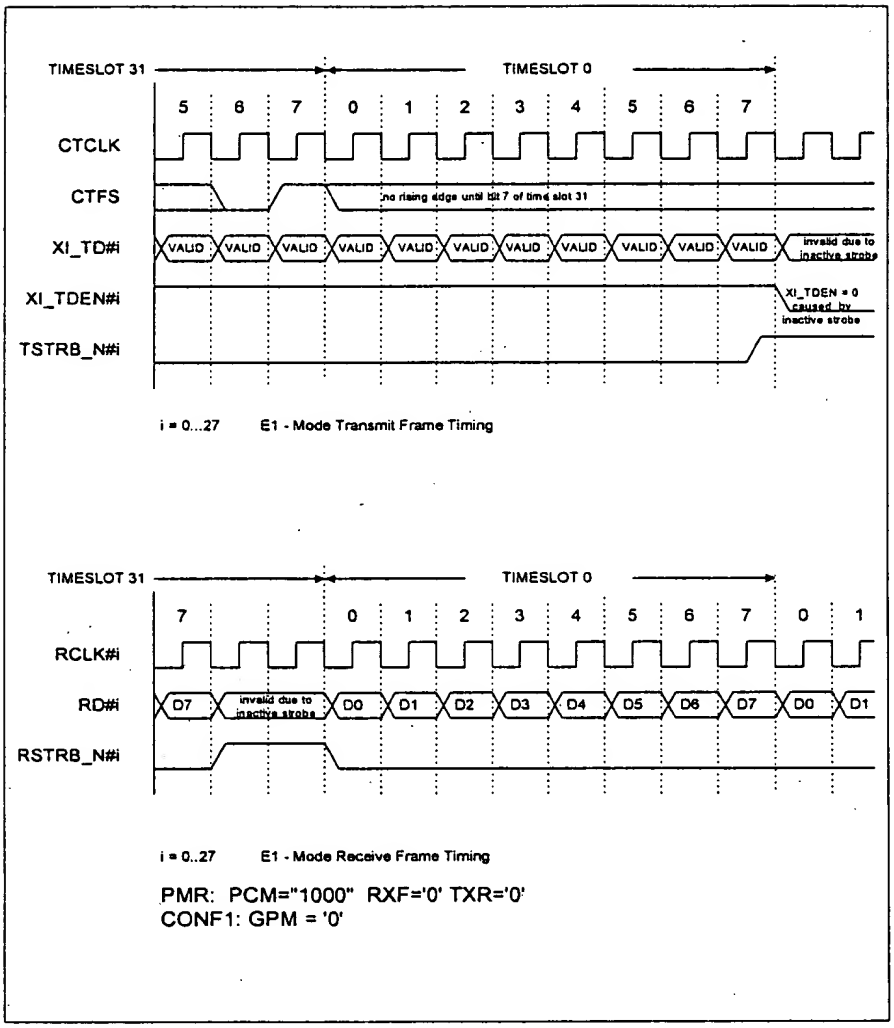


Figure 3.1.8.d

PCM interface timing for SCM: E1 with internal framing function (PMR.LT = 0, PMR.CTFSD = 0)

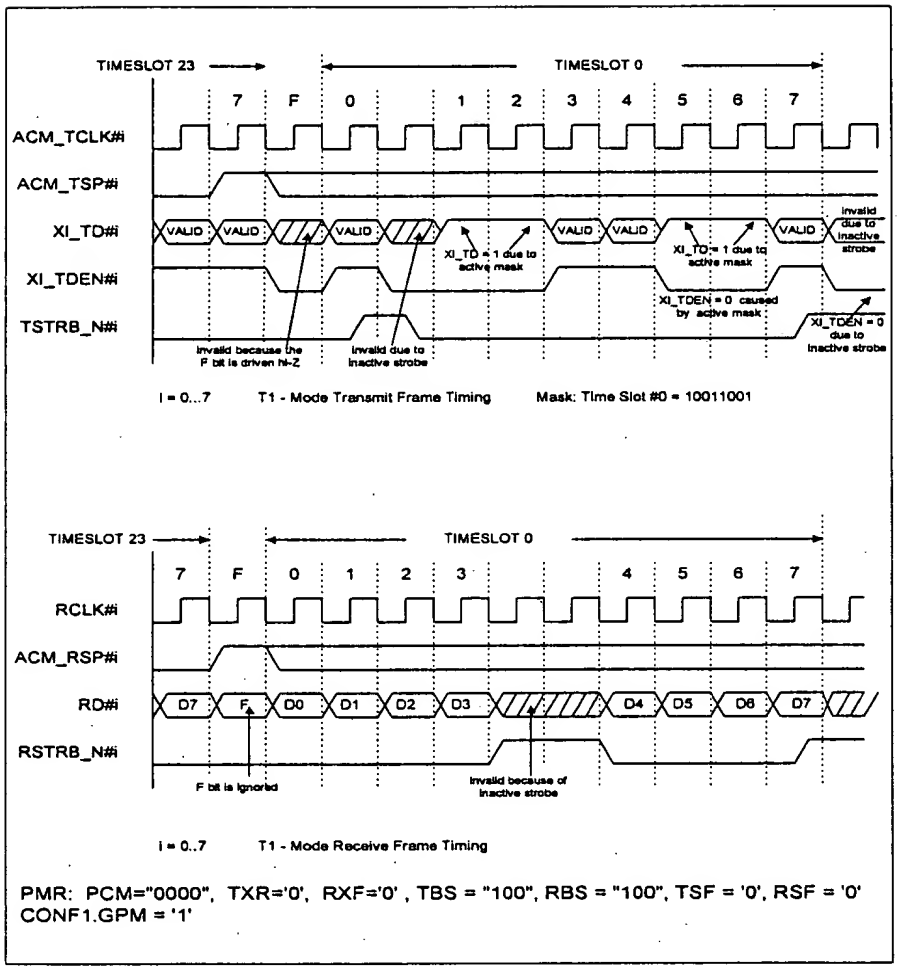


Figure 3.1.8e:

PCM interface timing for ACM: T1 without internal framing function

TBS = RBS = "100" corresponds to bit shift = 0 (s. PMR register)

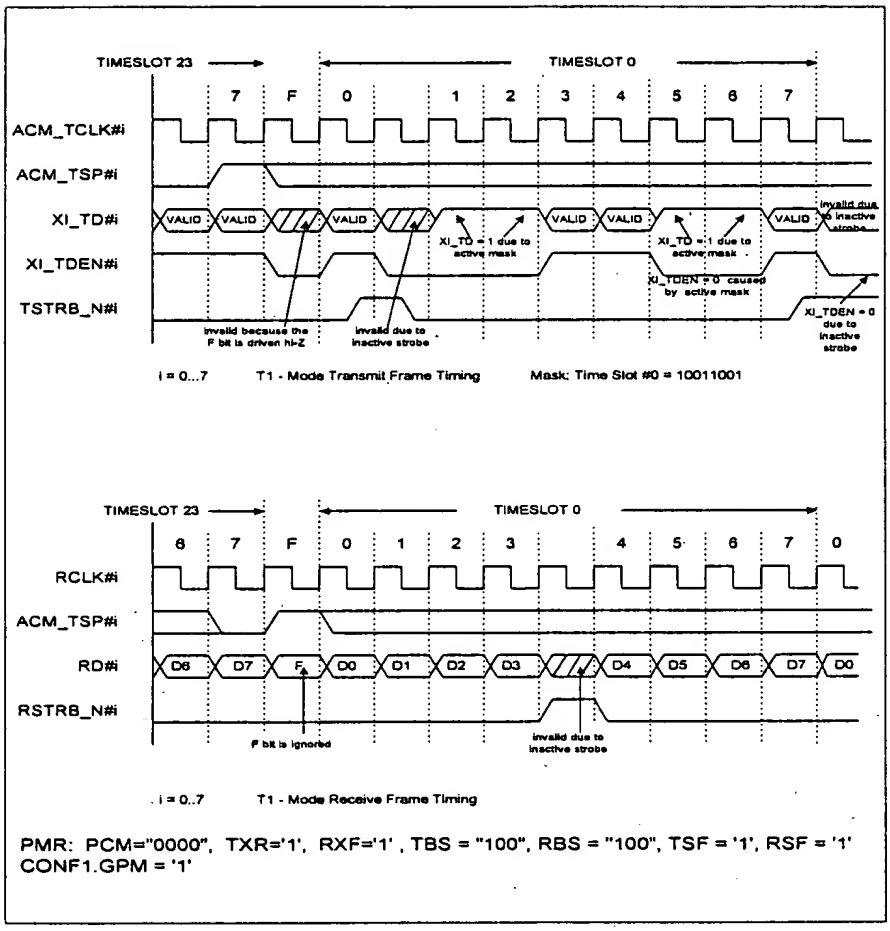


Figure 3.1.8f

PCM interface timing for ACM: T1 without internal framing function

Port mode register (PMR): RXF = 1, TXR = 1

Transmit: generation of transmit data at rising ACM_TCLK edge, sampling of the transmit sync pulse ACM_TSP at falling edge, sampling of the transmit strobe TSTRB_N at rising edge (TSTRB_N is expected to be provided half a clock cycle before the corresponding data are generated).

Receive: sampling of the receive data, receive sync pulse and receive strobe at falling RCLK edge.

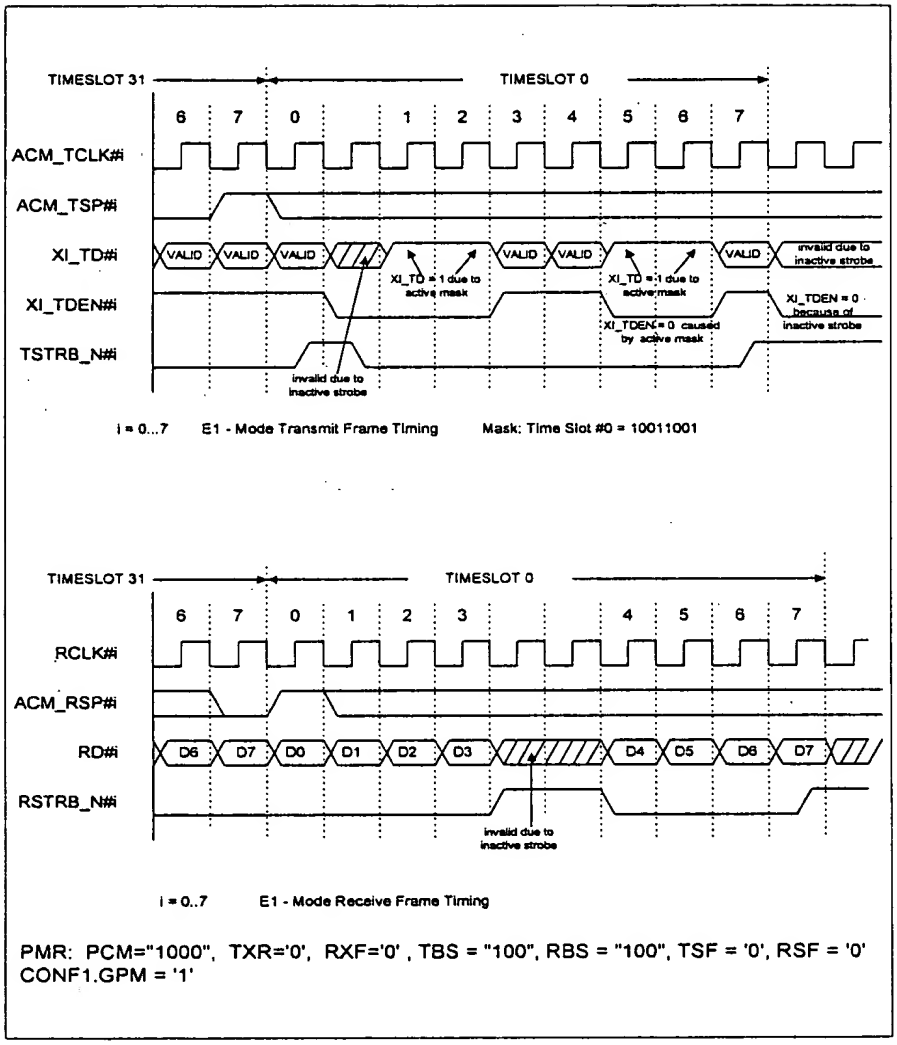


Figure 3.1.8.g

PCM interface timing for ACM: E1 without internal framing function

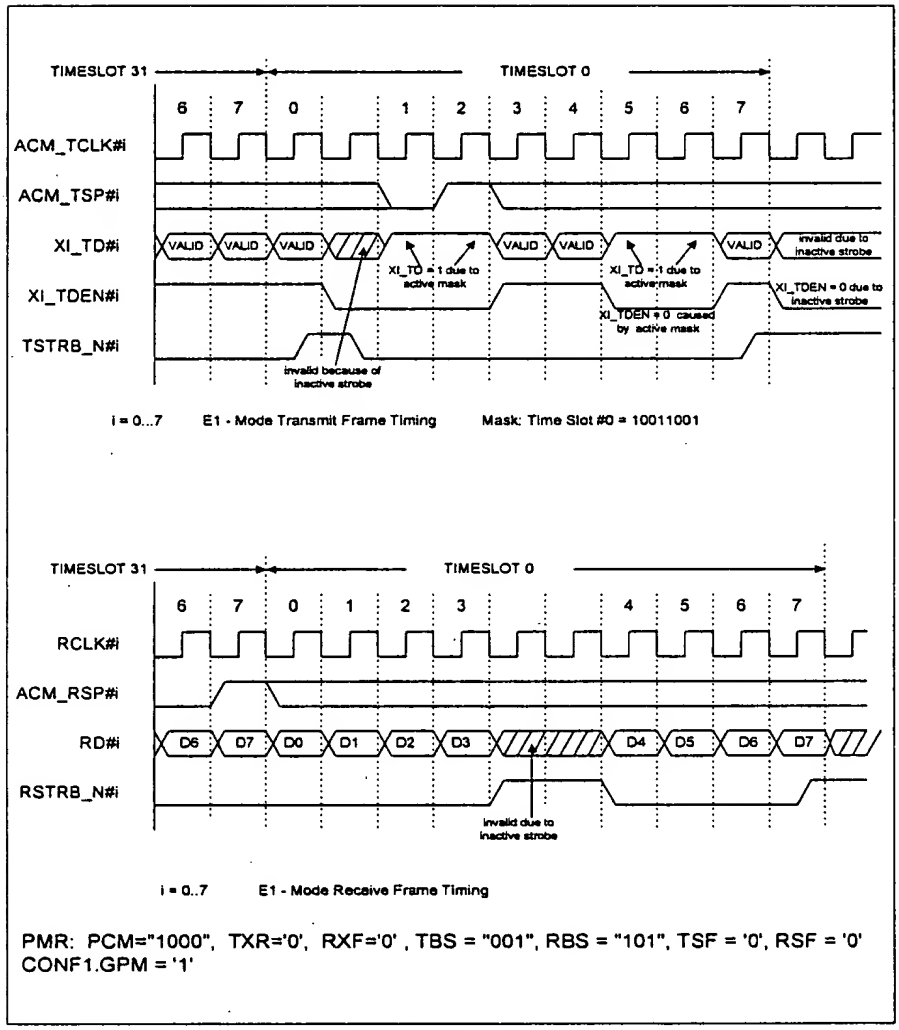


Figure 3.1.8.h

PCM interface timing for ACM: E1 without internal framing function

TBS = "001" corresponds to bit shift = -3 of the transmit data relative to the transmit sync pulse ACM_TSP

RBS = "101" corresponds to bit shift = +1 of the receive data relative to the receive sync pulse ACM_RSP

4 Register Description

4.1 Register Overview

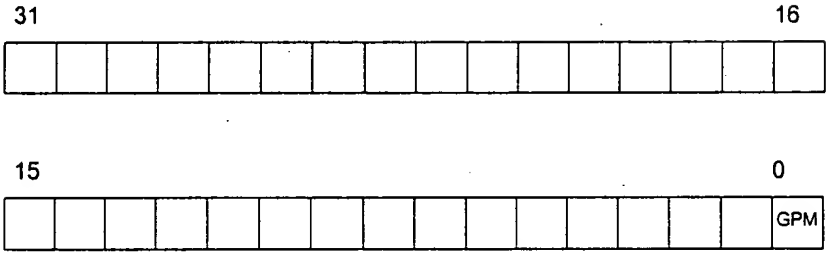
Register Overview Table : XPI V2.1

Register ID	Access	Absolute Address cs_n & a(7:2)	Reset Value	Comment
CONF1	R/W	40_H	00000000_H	(virtual global) configuration register 1
CONF2	R/W	44_H	00000000_H	(virtual global) configuration register 2
PMIAR	W	60_H	00000000_H	(macro specific) port mode indirect access register
PMR	R/W	64_H	$0104C000_H$	(macro specific) port mode register
REN	R/W	68_H	00000000_H	(macro specific) receive enable register
TEN	R/W	$6C_H$	00000000_H	(macro specific) transmit enable register

4.2 Detailed Register Description

4.2.1 (Virtual Global) Configuration Register 1(CONF1)

Access : read/write
Address : 00000040_H
Reset Value : 00000000_H



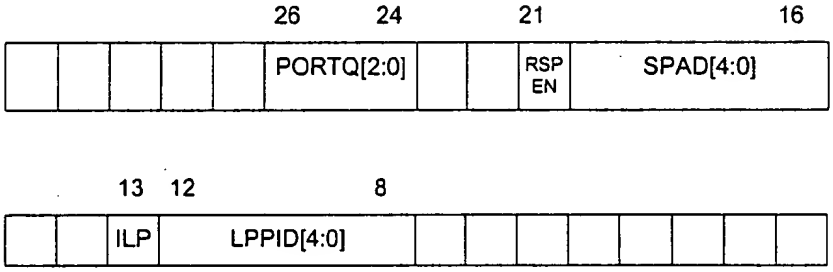
Note: This register is common for XPI and other macros. The macro XI just collect those data bits from the written dword (see above), that are relevant for macro XI. With a read access to this register, the macro XI drive only the value for the relevant bits. All other bits are set to '0'.

GPM: general PCM port mode:
'0' : standard channelized mode (SCM): 28 * T1 / E1 lines with chip internal framing function
'1': alternate channelized mode (ACM): 16* T1 / E1 lines lines (port 0...15) without chip internal framing function

Please note: M256_MODE = "00" forces the M256F in ACM mode

4.2.2 (Virtual Global) Configuration Register 2 (CONF2)

Access : read/write
Address : 00000044_H
Reset Value : 00000000_H

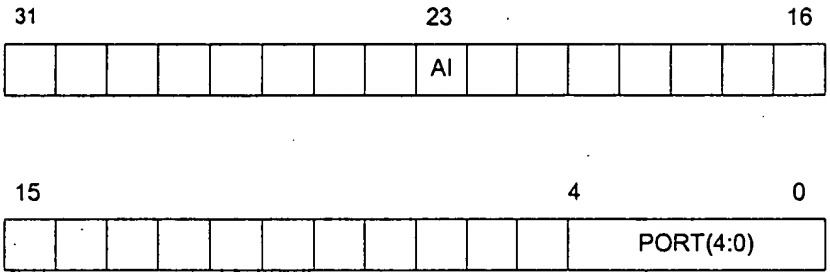


Note: This register is common for XPI and other macros. The macro XI just collect those data bits from the written dword (see above), that are relevant for macro XI. With a read access to this register, the macro XI drive only the value for the relevant bits. All other bits are set to '0'.

LPPID[4:0]:	port selection for internal portwise loop
ILP:	internal portwise loop on port selected by LPPID[4:0]
SPAD[4:0]	port selection for signaling the receive sync information provided by the on chip framer on pin RSPO_TCLKO (relevant in SCM mode only)
RSPEN:	if set to '1', the regenerated framer sync pulse is visible on RSPO_TCLKO if reset to '0', the effective transmit clock of port#0 is visible on RSPO_TCLKO
PORTQ[2:0]:	port interrupts will be written into this queue

4.2.3 Port Mode Indirect Access Register (PMIAR)

Access : write
Address : 00000060_H
Reset Value : 00000000_H



Note: This register is implemented once for all ports in the XPI

PORT[4:0]: Port number, to/from which the data in register PMR is written/read

AI: autoincrement mode, if set to '1' when writing the PMIAR, the port number bit field is automatically incremented after each write or read access to the data register PMR. The port number will wrap automatically at the maximum port number (M256F: port# 27)

4.2.4 Port Mode Register (PMR)

Access : read/write
Address : 00000064_H
Reset Value : $0104C000_H$

31	28			ACM				ACM
PCM[3:0]	0	0	0	TBS[2:0]	0	0	0	RBS[2:0]

15				ACM	ACM		7								0
REIM	TEIM	RXF	TXR	RSF	TSF	CTFSD	LT	0	0	0	0	0	0	0	0

Note: This register is available for each port (register bits labeled by "ACM" exist physically only for ports0...15, in contrast to the remaining bits that exist for each of the 28 ports)

PCM(3:0):

0000	T1 / 1.544MHz
1000	E1 / 2.048MHz
1111	Unchannelized

TSF, RSF '0': sample TSP/RSP at rising edge
'1': sample TSP/RSP at falling edge
(don't care for SCM)

TXR '0': transmitting TX data at falling edge, sampling TSTRB_N at falling edge, sampling CTFS in SCM mode at rising edge
'1': transmitting TX data at rising edge, sampling TSTRB_N at rising

edge, sampling CTFS in SCM mode at falling edge
(TXR must be programmable also for SCM !)

RXF '0': sampling RX data and TSTBR_N at rising edge
'1': sampling RX data and RSTRB_N at falling edge
(RXF must be programmable also for SCM !)

TEIM: transmit sync Error Interrupt Mask (reset value = '1')

REIM: receive sync Error Interrupt Mask (reset value = '1')

TBS, RBS : bit shift offset of +3bits/- 4bits **(don't care for SCM)**
Note: If an internal loop is active, RBS must be identical to TBS!!

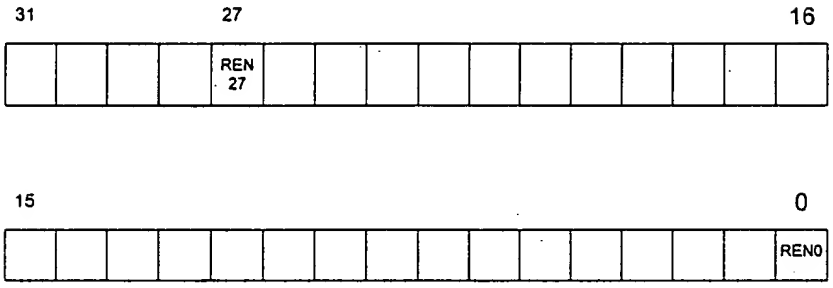
Bit24	Bit23	Bit22	shift of TD bit relative to TSP	Bit18	Bit17	Bit16	shift of RD bit relative to RSP
0	0	0	-4	0	0	0	-4
0	0	1	-3	0	0	1	-3
0	1	0	-2	0	1	0	-2
0	1	1	-1	0	1	1	-1
1	0	0	0	1	0	0	0
1	0	1	1	1	0	1	1
1	1	0	2	1	1	0	2
1	1	1	3	1	1	1	3

LT: if set to '1', the clock source of the serial transmit part is switched to RCLK

CTFSD: if set to '1', CTFS is ignored as external synchronization signal for transmit frames in SCM mode

4.2.5 Receive Enable Register (REN)

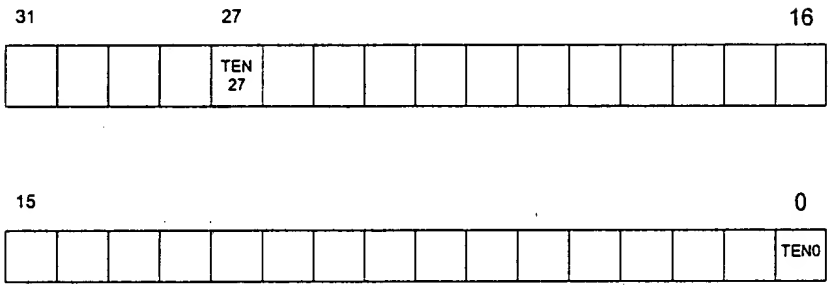
Access	: read/write
Address	: 00000068_H
Reset Value	: 00000000_H



REN[27:0]: if set to '1', the corresponding receive port is enabled, i.e. incoming data is processed. After synchronization is achieved, the XPI requests service from the TSAR for further data processing.
If set to '0', no requests are forwarded to FRAMR and TSAR.

4.2.6 Transmit Enable Register (TEN)

Access	: read/write
Address	: $0000006C_H$
Reset Value	: 00000000_H



TEN[27:0]: if set to '1', the corresponding transmit port is enabled, i. e. sends data originating from PMT if the corresponding timeslot is also enabled in TSAT.
If set to '0', the corresponding output port is Hi-Z generally and no requests are forwarded to FRAMT and TSAT.